46. [Amended] The method of claim 43[, further comprising] wherein:

forming a source region comprises forming a source region and a drain region in [the] a silicon substrate [and] that are separated by a channel region in the silicon substrate; and

further comprising:

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

47. [Amended] The method of claim 43[, further comprising] wherein:

forming a source region comprises forming a source region and a drain region in [the] a silicon substrate [and] that are separated by a channel region in the silicon substrate; and

further comprising:

oxidizing the gate by plasma oxidation to form an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

50. [Twice Amended] A method of fabricating a transistor comprising:

forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

forming an insulating layer on [a] the silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation; and

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the silicon substrate.

53. [Amended] The method of claim 50, further comprising:

[forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate;]

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

54. [Amended] The method of claim 50, further comprising:

[forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate;]

oxidizing the gate by plasma oxidation to form an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

55. [Twice Amended] A method of fabricating a transistor comprising:

<u>forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;</u>

forming an insulating layer on [a] <u>the</u> silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation; and

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the <u>silicon</u> substrate.

58. [Amended] The method of claim 55, further comprising:

[forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate;]

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

59. [Amended] The method of claim 55, further comprising:

[forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate;]

oxidizing the gate by plasma oxidation to form an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

60. [Twice Amended] A method of fabricating a floating gate transistor comprising:

forming a source region and a drain region in a substrate that are separated by a channel region in the substrate;

forming an insulating layer on [a] the substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric.

62. [Twice Amended] The method of claim 60, further comprising:

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming a source region comprises forming a source region and a drain region in [the] a silicon substrate [and] that are separated by a channel region in the substrate; [and]

wherein forming an insulating layer comprises forming a layer of tunnel oxide on [a] the silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.

65. [Twice Amended] A method of fabricating a floating gate transistor comprising:

<u>forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;</u>

forming an insulating layer on [a] <u>the</u> silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the silicon substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric.

67. [Twice Amended] The method of claim 65, further comprising:

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; <u>and</u>

[forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate; and]

wherein forming an insulating layer comprises forming a layer of tunnel oxide on [a] <u>the</u> silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.

68. [Twice Amended] A method of fabricating a memory cell comprising:

<u>forming a source region and a drain region in a substrate that are separated by a channel region in the substrate;</u>

forming an insulating layer on [a] <u>the</u> substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric <u>that is coupled to receive a control voltage from a memory device</u>.

70. [Twice Amended] The method of claim 68, further comprising:

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming a source region comprises forming a source region and a drain region in [the] a silicon substrate [and] that are separated by a channel region in the silicon substrate; [and]

wherein forming an insulating layer comprises forming a layer of tunnel oxide on [a] the silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric that is coupled to receive a programming voltage or a read voltage from a memory device.

73. [Twice Amended] A method of fabricating a memory cell comprising:

forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

forming an insulating layer on [a] the silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation;

removing portions of the insulating layer and the layer of the silicon carbide compound

$Si_{1-x}C_x$ to form a floating gate on the silicon substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric <u>that is coupled to receive a control voltage from a memory device</u>.

75. [Twice Amended] The method of claim 73, further comprising:

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; <u>and</u>

[forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate; and]

wherein forming an insulating layer comprises forming a layer of tunnel oxide on [a] <u>the</u> silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric <u>that is coupled to receive a programming voltage or a read voltage from a memory device</u>.